ECEN4243

LAB 0

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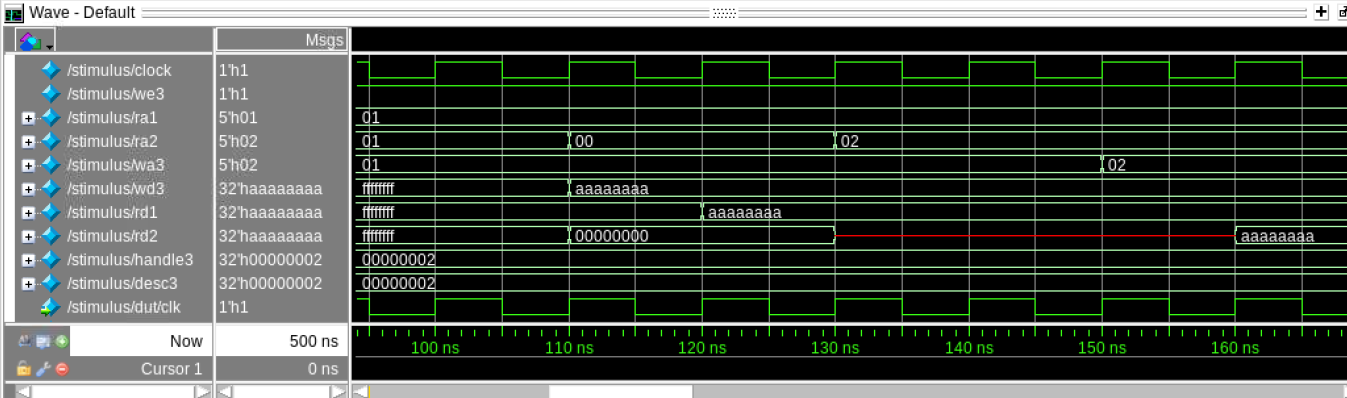
https://github.com/jordanpaul98/ECEN4243\_CompARC/tree/main/LAB\_0

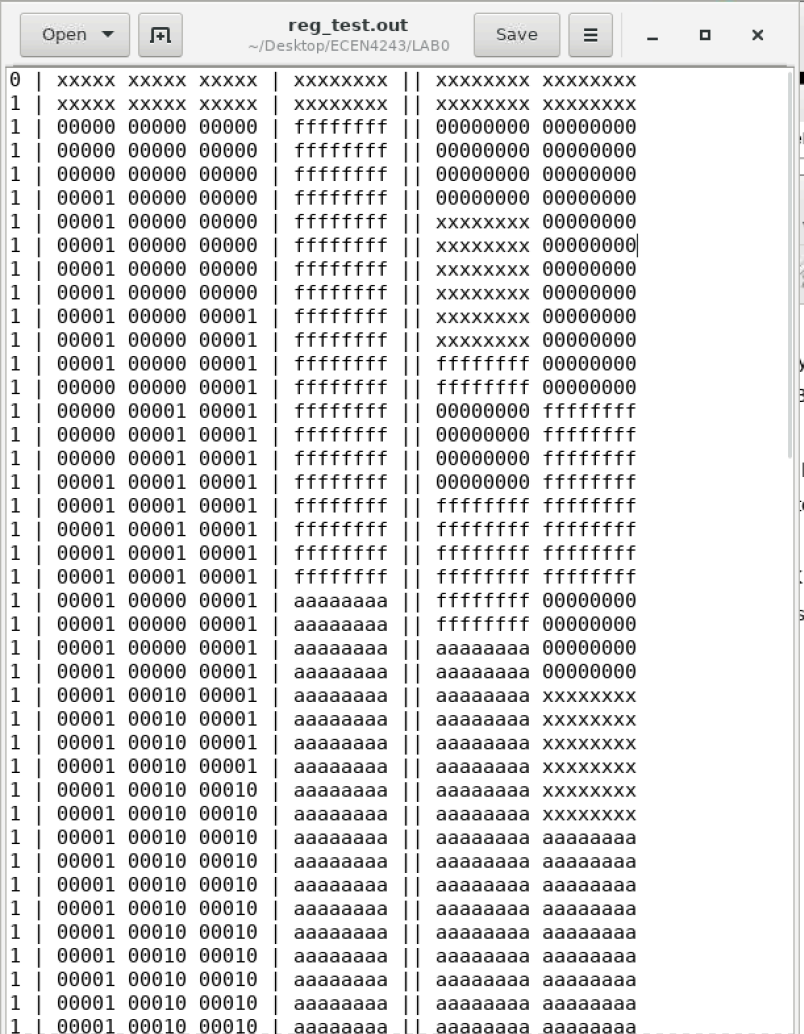
files:

* FSM.do, FSM.sv, FSM\_tb.sv
* regfile.sv
* regfile.do, regfile\_tb.sv
* regfile\_testbench.do, regfile\_testbench.sv, regfile.tv
* regfile\_gen.py

**Run: vsim -do regfile.do**

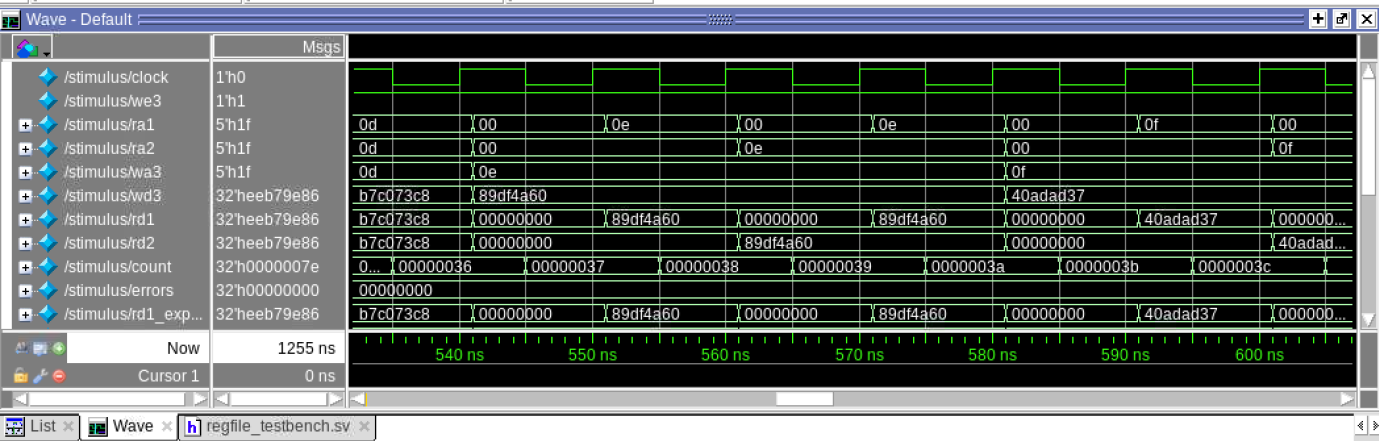
* test bench uses Case with pre enter cases to test the regfile.sv
  + outputs test to reg\_test.out
* general test cases, exploring the functionality of the registers and operations

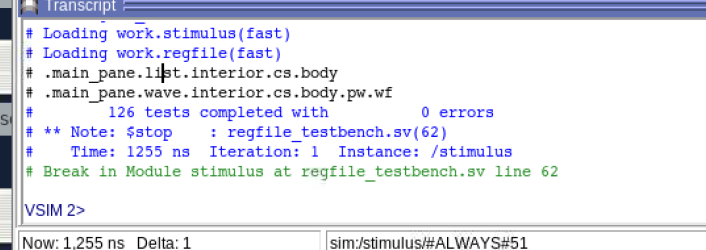




**Run: vsim -do regfile\_testbench.do**

* test bench using test vectors loaded in from regfile.tv generated from regfile\_gen.py
* testes every register state (126) testes (minus 2 duplicated test cases)
  + testes = (2 ^ num\_registers) \* (2 ^ register\_bits)
* will print error message if a test failed on which line number test it failed on.





Test vectors input (112 bits)

